

# 74LVC544A

Octal D-type registered transceiver; inverting; 3-state

Rev. 03 — 11 May 2004

Product data sheet

## 1. General description

The 74LVC544A is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74LVC544A is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable inputs ( $\overline{LEAB}$  and  $\overline{LEBA}$ ) and output enable inputs ( $\overline{OEAB}$  and  $\overline{OEBA}$ ) are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC544A contains eight D-type latches, with separate inputs and controls for each set. For data flow from pins A to B, for example, the A to B enable input (pin  $\overline{EAB}$ ) must be LOW in order to enter data from pins A0 to A7 or take data from pins B0 to B7. With pin  $\overline{EAB}$  LOW, a LOW signal on the A to B latch enable input (pin  $\overline{LEAB}$ ) makes the A to B latches transparent; a subsequent LOW-to-HIGH transition on pin  $\overline{LEAB}$  puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With pins  $\overline{EAB}$  and  $\overline{OEAB}$  both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

## 2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B/JESD36
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Supports partial power-down applications; inputs/outputs are high-impedance when  $V_{CC} = 0$  V
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C.

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### 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$ , $t_{PLH}$	propagation delay $\overline{A_n}$ to $\overline{B_n}$ ; $\overline{B_n}$ to $\overline{A_n}$	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	-	3.6	-	ns
$C_I$	input capacitance		-	5.0	-	pF
$C_{I/O}$	input/output capacitance		-	4.0	-	pF
$C_{PD}$	power dissipation capacitance per latch	$V_{CC} = 3.3\text{ V}$				
		outputs enabled	-	16.0	-	pF
		outputs disabled	-	4.0	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2] The condition is  $V_I = GND$  to  $V_{CC}$ .

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74LVC544AD	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC544ADB	-40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC544APW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

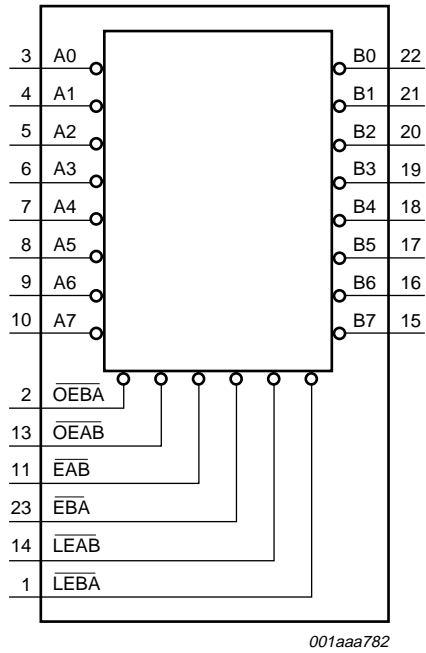


Fig 1. Logic symbol.

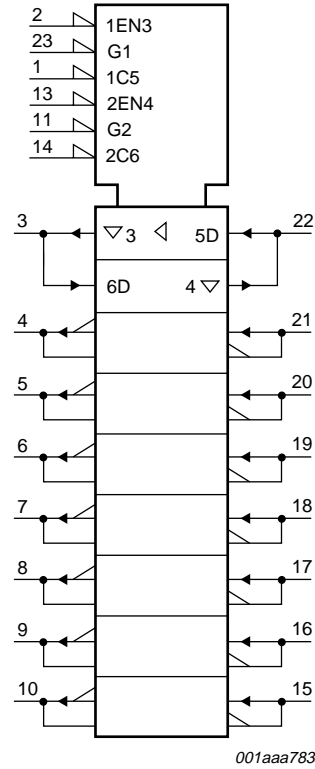


Fig 2. IEC logic symbol.

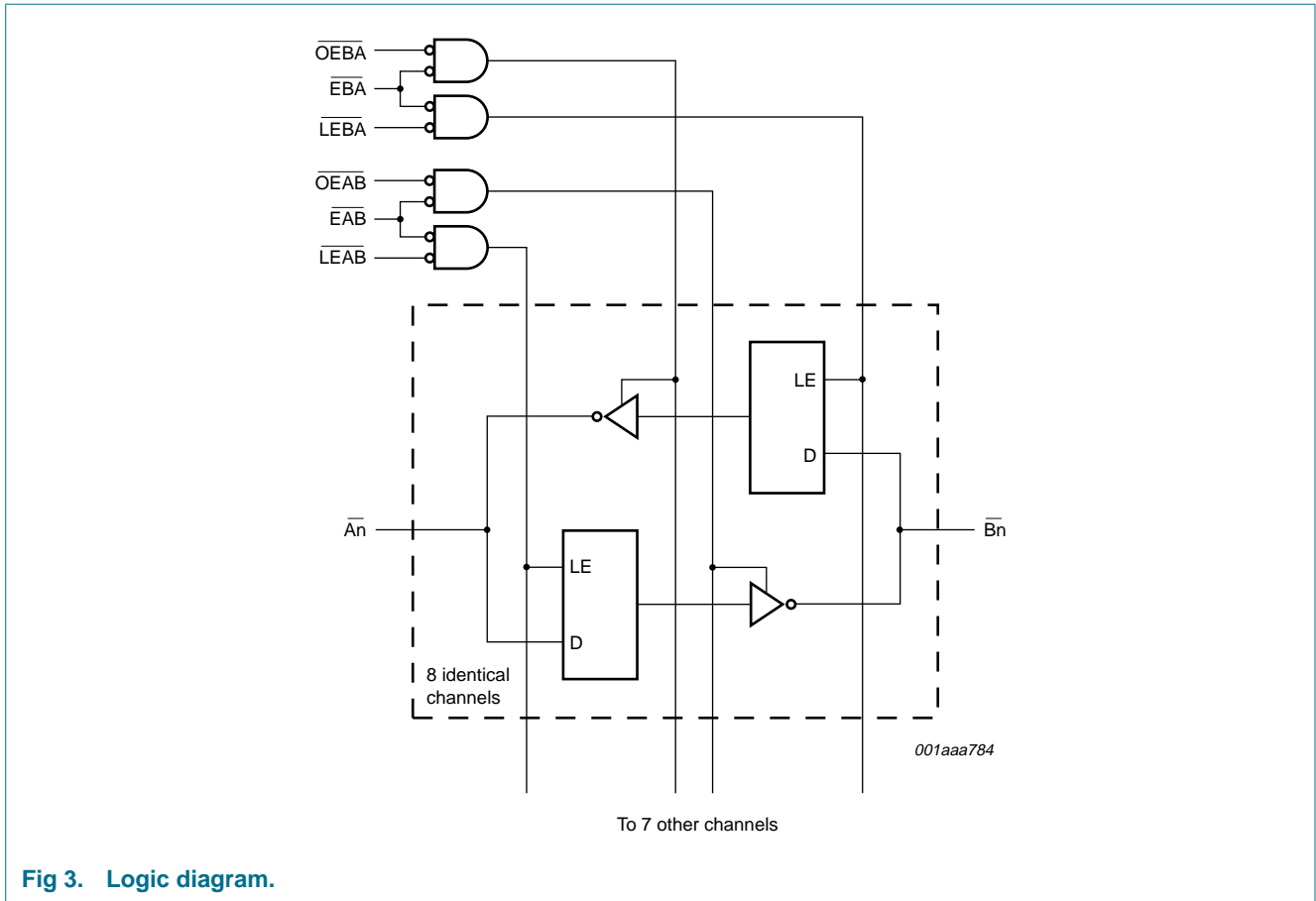


Fig 3. Logic diagram.

## 6. Pinning information

### 6.1 Pinning

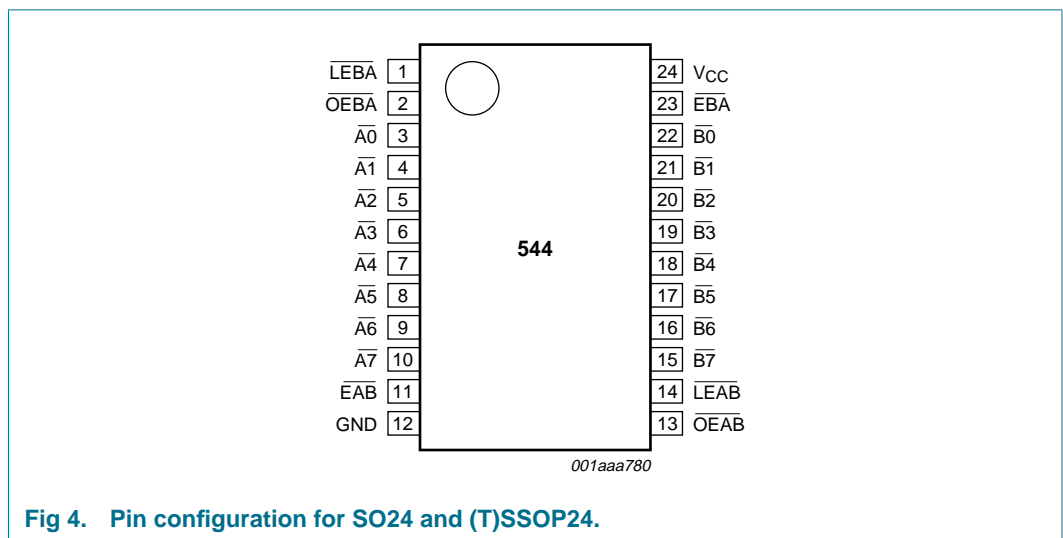


Fig 4. Pin configuration for SO24 and (T)SSOP24.

## 6.2 Pin description

Table 3: Pin description

Pin	Symbol	Description
1	$\overline{\text{LEBA}}$	B to A latch enable input (active LOW)
2	$\overline{\text{OEBA}}$	B to A output enable input (active LOW)
3	$\overline{\text{A0}}$	A data input or output
4	$\overline{\text{A1}}$	A data input or output
5	$\overline{\text{A2}}$	A data input or output
6	$\overline{\text{A3}}$	A data input or output
7	$\overline{\text{A4}}$	A data input or output
8	$\overline{\text{A5}}$	A data input or output
9	$\overline{\text{A6}}$	A data input or output
10	$\overline{\text{A7}}$	A data input or output
11	$\overline{\text{EAB}}$	A to B enable input (active LOW)
12	GND	ground (0 V)
13	$\overline{\text{OEAB}}$	A to B output enable input (active LOW)
14	$\overline{\text{LEAB}}$	A to B latch enable input (active LOW)
15	$\overline{\text{B7}}$	B data output or input
16	$\overline{\text{B6}}$	B data output or input
17	$\overline{\text{B5}}$	B data output or input
18	$\overline{\text{B4}}$	B data output or input
19	$\overline{\text{B3}}$	B data output or input
20	$\overline{\text{B2}}$	B data output or input
21	$\overline{\text{B1}}$	B data output or input
22	$\overline{\text{B0}}$	B data output or input
23	$\overline{\text{EBA}}$	B to A enable input (active LOW)
24	V <sub>CC</sub>	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table <sup>[1]</sup>

Operating mode	Input				Output
	OEXX	EXX	LEXX	data	
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled plus latch	L	↑	L	h	Z
	L	↑	L	l	Z
Latch plus display	L	L	↑	h	L
	L	L	↑	l	H

Table 4: Function table [1]

Operating mode	Input				Output
	OEXX	EXX	LEXX	data	
Transparent	L	L	L	H	L
	L	L	L	L	H
Hold (do nothing)	L	L	H	X	NC

- [1] XX = AB for A to B direction and BA for B to A direction;  
 H = HIGH voltage level;  
 L = LOW voltage level;  
 h = HIGH state must be present one set-up time before the LOW-TO-HIGH transition of  $\overline{LEAB}$ ,  $\overline{LEBA}$ ,  $\overline{EAB}$  and  $\overline{EBA}$ ;  
 l = LOW state must be present one set-up time before the LOW-TO-HIGH transition of  $\overline{LEAB}$ ,  $\overline{LEBA}$ ,  $\overline{EAB}$  and  $\overline{EBA}$ ;  
 X = don't care;  
 ↑ = LOW-TO-HIGH level transition;  
 NC = no change;  
 Z = high-impedance OFF-state.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$ V	-	-50	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	output HIGH or LOW state	[1] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[1] -0.5	+6.5	V
$I_O$	output source or sink current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] For SO24 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.  
 For T(SSOP)24 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
$V_I$	input voltage		0	-	5.5	V

Table 6: Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	-	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C [1]</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	GND	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	[2] V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	[2] -	GND	0.2	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	-	±0.1	±5	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	[3] -	0.1	±10	μA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 3.6 V; I <sub>O</sub> = 0 A	-	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>O</sub> = 0 A	[2] -	5	500	μA
C <sub>I</sub>	input capacitance		-	5.0	-	pF
C <sub>I/O</sub>	input/output capacitance		-	4.0	-	pF
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.75	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 1	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.3	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	-	-	±20	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	[3]	-	±20	μA
I <sub>off</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0 V	-	-	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 3.6 V; I <sub>O</sub> = 0 A	-	-	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>O</sub> = 0 A	-	-	5000	μA

[1] All typical values are measured T<sub>amb</sub> = 25 °C.

[2] These typical values are measured at V<sub>CC</sub> = 3.3 V.

[3] For transceivers, the parameter I<sub>OZ</sub> includes the input leaking current.

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

GND = 0 V; see [Figure 9](#) for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C [1]</b>						
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay $\overline{A_n}$ to $\overline{B_n}$ ; $\overline{B_n}$ to $\overline{A_n}$	see <a href="#">Figure 5</a>				
		V <sub>CC</sub> = 1.2 V	-	17	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	7.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[2]	1.0	3.6	6.5
	propagation delay $\overline{LEBA}$ to $\overline{A_n}$ ; $\overline{LEAB}$ to $\overline{B_n}$	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 1.2 V	-	19	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[2]	1.0	3.3	7.5



**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V; see Figure 9 for test circuit.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PZH}, t_{PZL}$	3-state output enable time $\overline{OEBA}$ to $\overline{An}$ ; $\overline{OEAB}$ to $\overline{Bn}$	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	18	-	ns
		$V_{CC} = 2.7\text{ V}$	1.5	-	9.5	ns
	3-state output enable time $\overline{EBA}$ to $\overline{An}$ ; $\overline{EAB}$ to $\overline{Bn}$	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	20	-	ns
		$V_{CC} = 2.7\text{ V}$	1.5	-	9.9	ns
	3-state output disable time $\overline{OEBA}$ to $\overline{An}$ ; $\overline{OEAB}$ to $\overline{Bn}$	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	8.0	-	ns
		$V_{CC} = 2.7\text{ V}$	1.5	-	7.5	ns
	3-state output disable time $\overline{EBA}$ to $\overline{An}$ ; $\overline{EAB}$ to $\overline{Bn}$	see <a href="#">Figure 8</a>				
		$V_{CC} = 1.2\text{ V}$	-	9.0	-	ns
		$V_{CC} = 2.7\text{ V}$	1.5	-	7.9	ns
$t_W$	LEXX pulse with LOW	see <a href="#">Figure 6</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.7\text{ V}$	2.0	-	-	ns
$t_{su}$	set-up time $\overline{An}, \overline{Bn}$ to LEXX; $\overline{An}, \overline{Bn}$ to EXX	see <a href="#">Figure 7</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.7\text{ V}$	2.0	-	-	ns
$t_h$	hold time $\overline{An}, \overline{Bn}$ to LEXX; $\overline{An}, \overline{Bn}$ to EXX	see <a href="#">Figure 7</a>				
		$V_{CC} = 1.2\text{ V}$	-	-	-	ns
		$V_{CC} = 2.7\text{ V}$	1.0	-	-	ns
$t_{sk(0)}$	skew		[3]	-	-	1.0 ns
$C_{PD}$	power dissipation capacitance per latch	$V_{CC} = 3.3\text{ V}$	[4]	[5]		
		outputs enabled	-	16.0	-	pF
		outputs disabled	-	4.0	-	pF

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V; see Figure 9 for test circuit.*

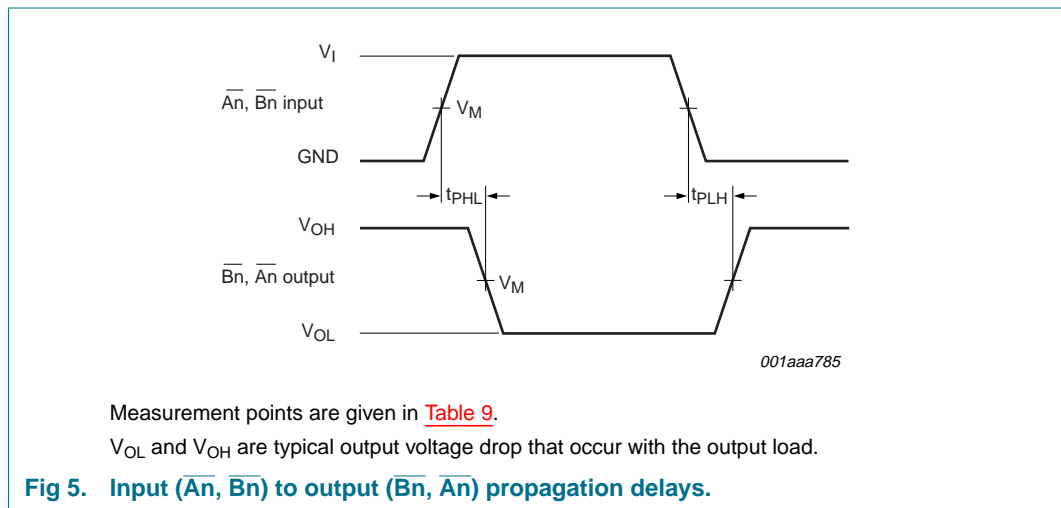
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay $\overline{A}_n$ to $\overline{B}_n$ ; $\overline{B}_n$ to $\overline{A}_n$	see <a href="#">Figure 5</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	9.5	ns
	propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$ ; $\overline{LE}_{AB}$ to $\overline{B}_n$	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	11.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	-	8.5	ns
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	12.0	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	3-state output enable time $\overline{OEBA}$ to $\overline{A}_n$ ; $\overline{OEAB}$ to $\overline{B}_n$	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	12.0	ns
	3-state output enable time $\overline{EBA}$ to $\overline{A}_n$ ; $\overline{EAB}$ to $\overline{B}_n$	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	12.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	-	11.5	ns
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	9.5	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	3-state output disable time $\overline{OEBA}$ to $\overline{A}_n$ ; $\overline{OEAB}$ to $\overline{B}_n$	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	9.5	ns
	3-state output disable time $\overline{EBA}$ to $\overline{A}_n$ ; $\overline{EAB}$ to $\overline{B}_n$	see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	10.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	-	9.0	ns
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	ns
t <sub>W</sub>	$\overline{LEXX}$ pulse with LOW	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	ns
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	ns
t <sub>su</sub>	set-up time $\overline{A}_n$ , $\overline{B}_n$ to $\overline{LEXX}$ ; $\overline{A}_n$ , $\overline{B}_n$ to $\overline{EXX}$	see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	ns
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.0	-	-	ns
t <sub>h</sub>	hold time $\overline{A}_n$ , $\overline{B}_n$ to $\overline{LEXX}$ ; $\overline{A}_n$ , $\overline{B}_n$ to $\overline{EXX}$	see <a href="#">Figure 7</a>				
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.0	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	-	-	ns
		V <sub>CC</sub> = 1.2 V	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	-	ns
t <sub>sk(0)</sub>	skew		[3]	-	-	1.5 ns

[1] All typical values are measured T<sub>amb</sub> = 25 °C.

[2] These typical values are measured at V<sub>CC</sub> = 3.3 V.

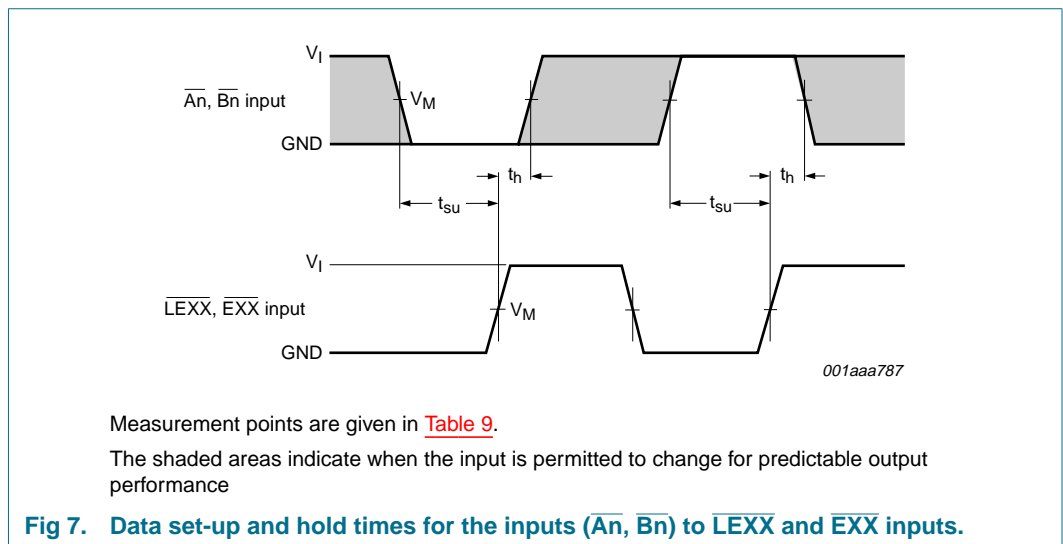
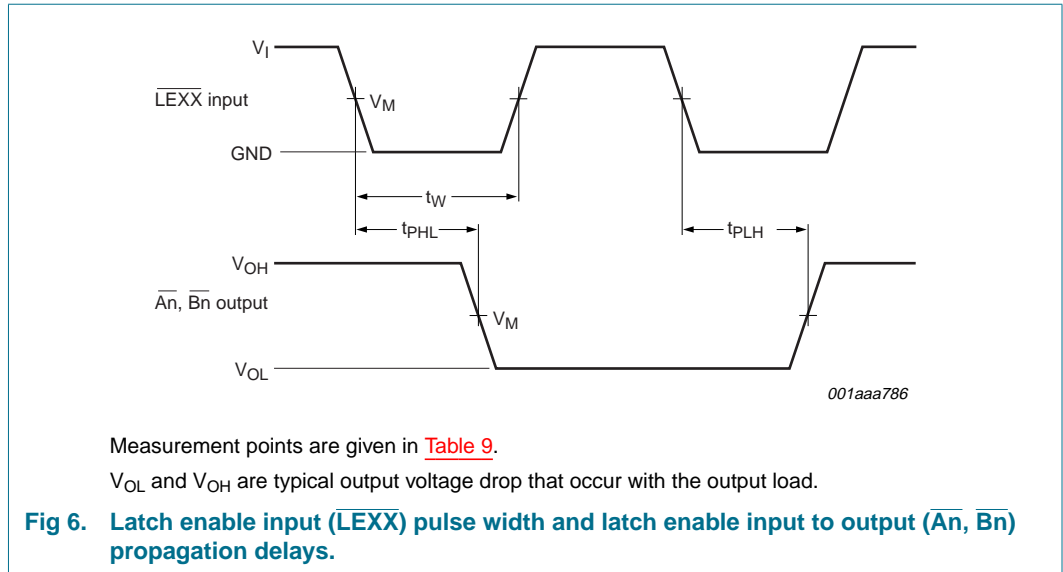
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = total load switching outputs;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- [5] The condition is  $V_I = GND$  to  $V_{CC}$ .

## 12. Waveforms



**Table 9: Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V



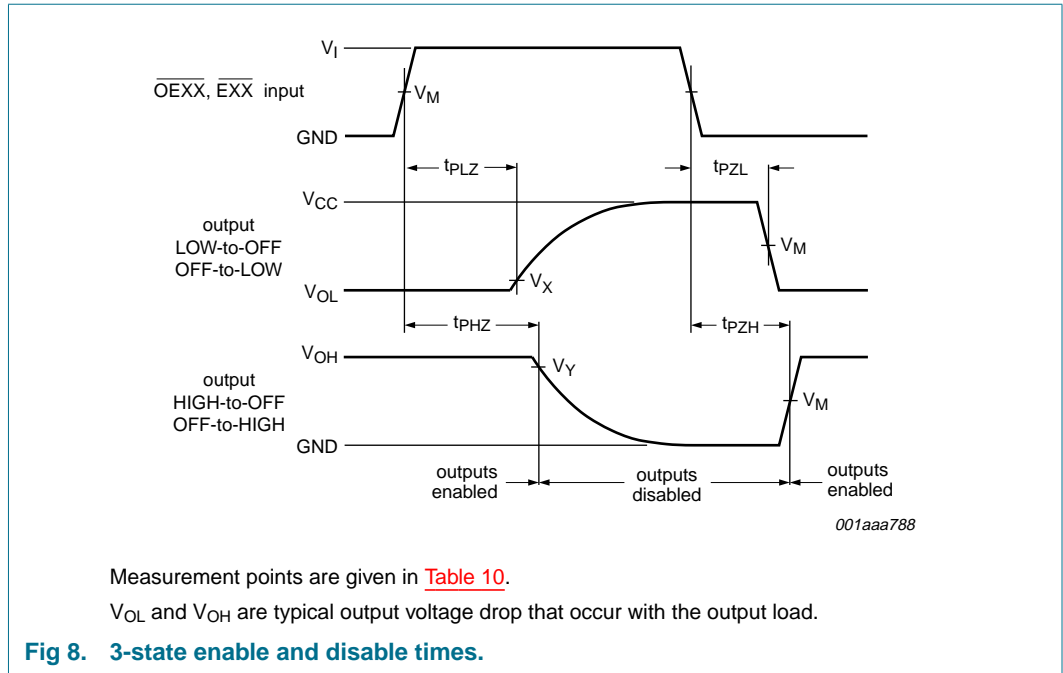
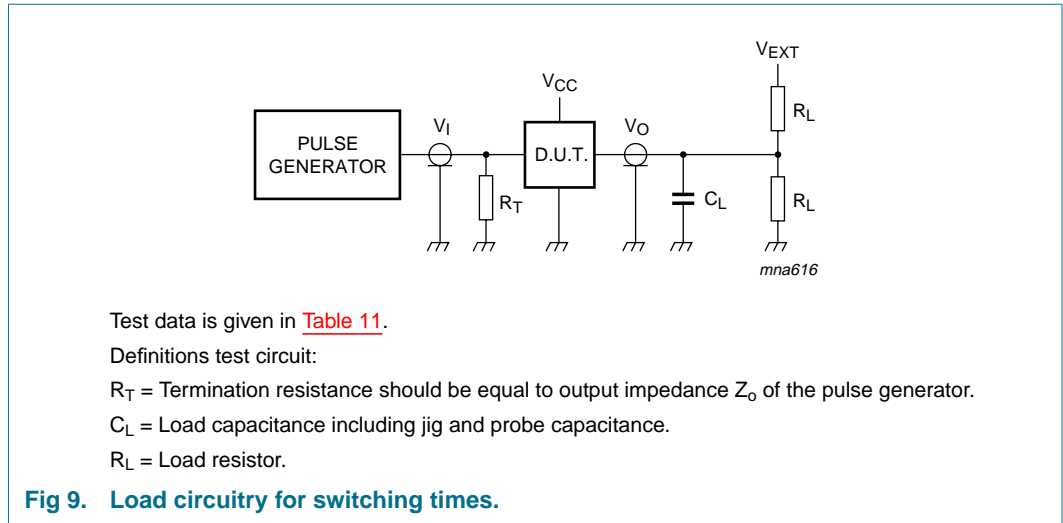


Table 10: Measurement points

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \text{ V}$	$V_{OH} - 0.1 \text{ V}$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



**Table 11: Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.2 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$ [1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$

[1] The circuit performs better when  $R_L = 1000 \Omega$ .

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

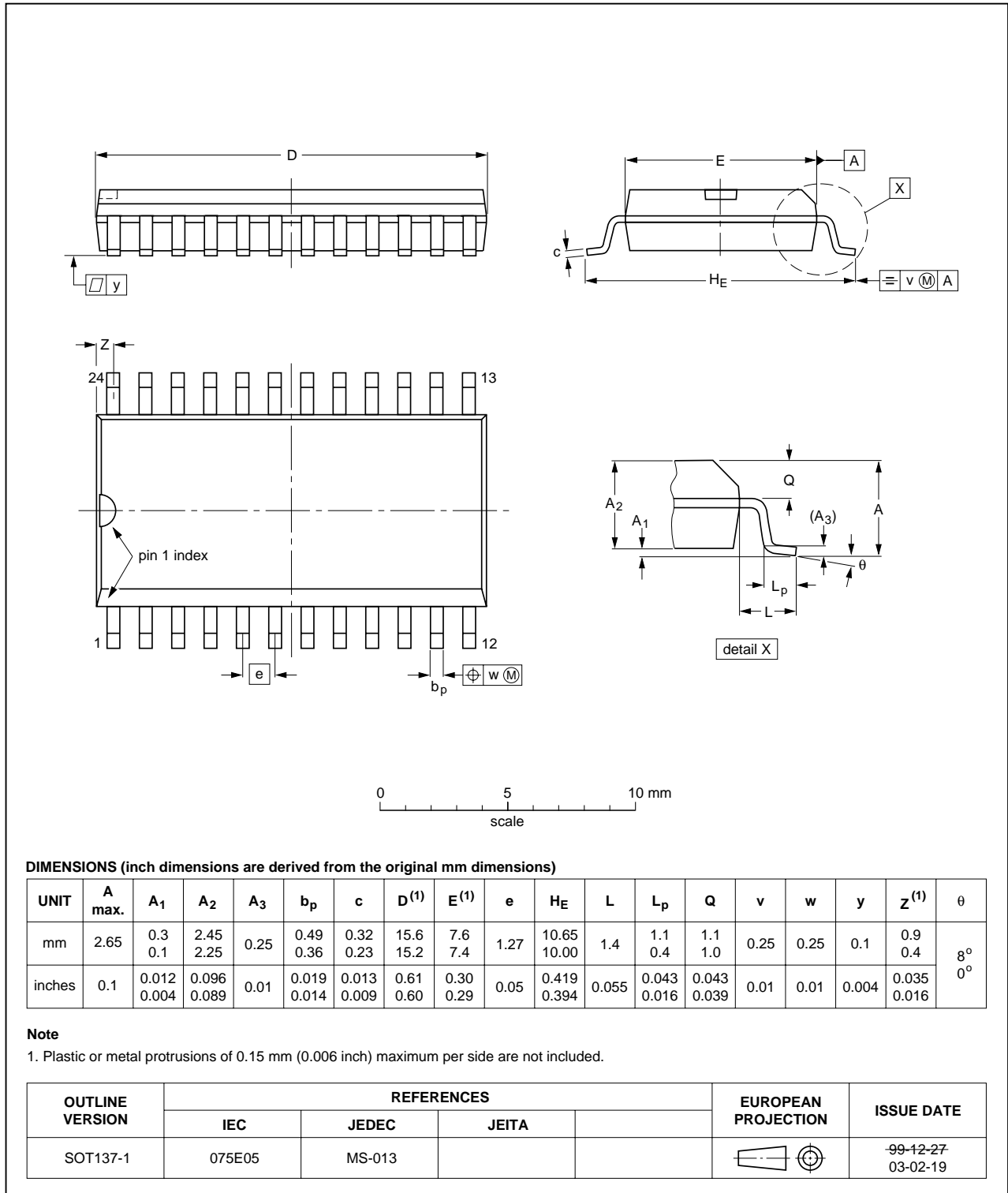


Fig 10. Package outline SO24.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

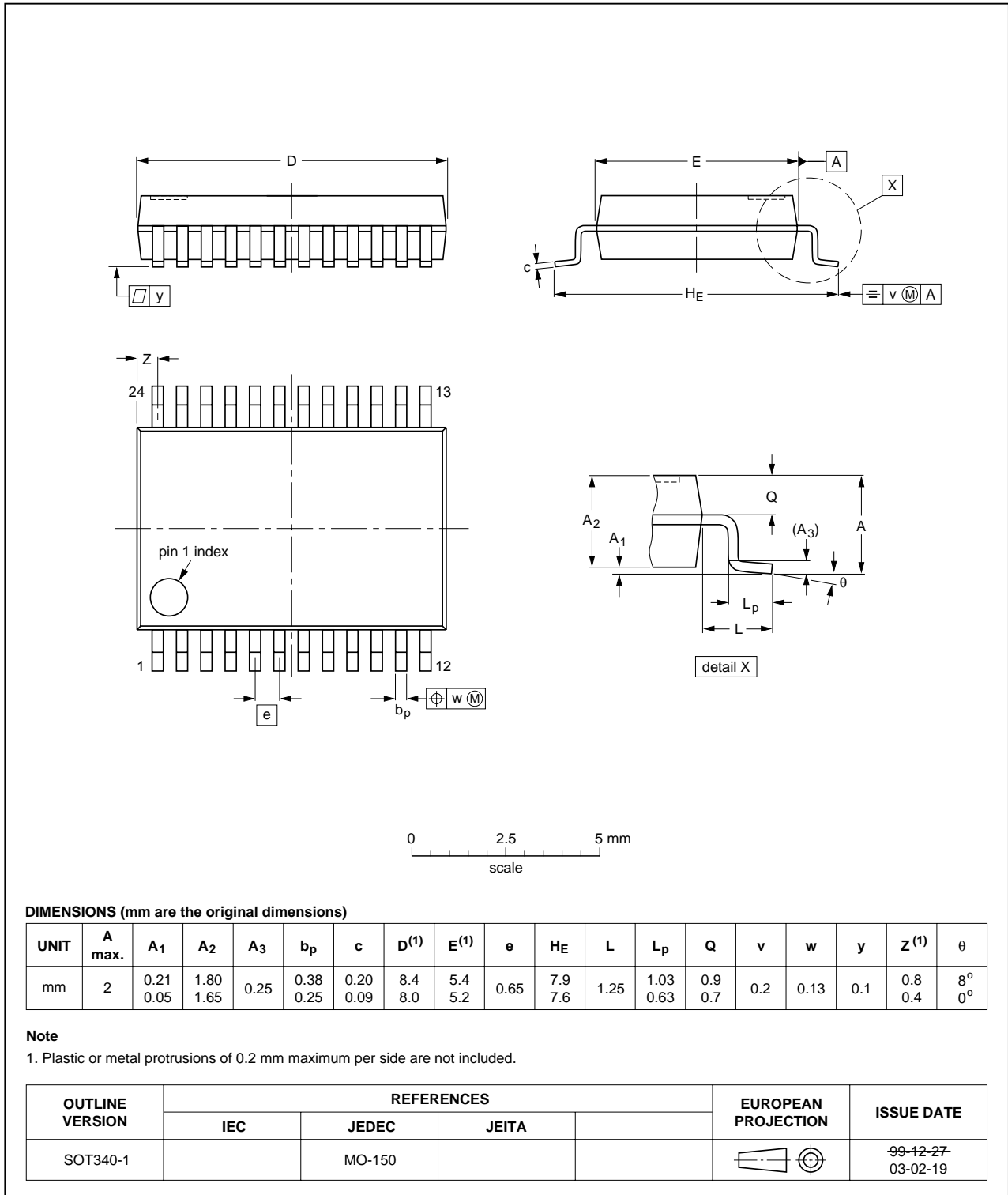


Fig 11. Package outline SSOP24.



TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

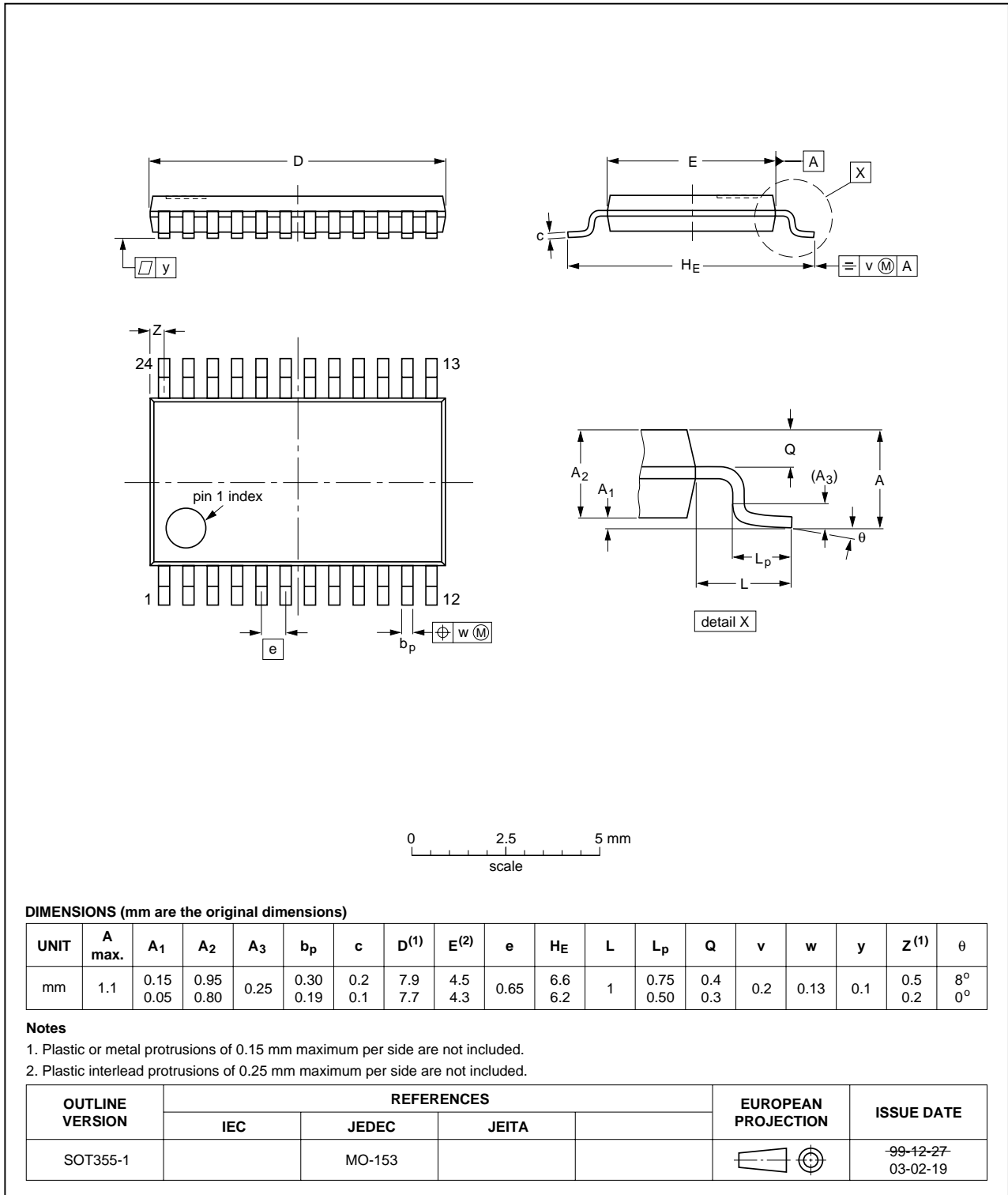


Fig 12. Package outline TSSOP24.

## 14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC544A_3	20040511	Product data	-	9397 750 13127	74LVC544A_2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors</li> <li>• <a href="#">Table 1</a>: updated various values</li> <li>• <a href="#">Table 7</a>: changed various values</li> <li>• <a href="#">Table 7</a>: added values for <math>T_{amb} = -40\text{ °C}</math> to <math>+125\text{ °C}</math></li> <li>• <a href="#">Table 8</a>: changed various values</li> <li>• <a href="#">Table 8</a>: added values for <math>T_{amb} = -40\text{ °C}</math> to <math>+125\text{ °C}</math>.</li> </ul>				
74LVC544A_2	19980729	Product specification	-	9397 750 04512	-

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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